

# CPC COOPERATIVE PATENT CLASSIFICATION

## H ELECTRICITY

(NOTE omitted)

### H10 SEMICONDUCTOR DEVICES; ELECTRIC SOLID-STATE DEVICES NOT OTHERWISE PROVIDED FOR

#### H10B ELECTRONIC MEMORY DEVICES

##### Volatile memory devices

##### **10/00 Static random access memory [SRAM] devices**

- 10/10 . SRAM devices comprising bipolar components

##### **WARNING**

Group [H10B 10/10](#) is incomplete pending reclassification of documents from groups [H01L 27/1027](#), [H01L 27/1028](#) and [H10B 99/00](#).

All groups listed in this Warning should be considered in order to perform a complete search.

- 10/12 . {comprising a MOSFET load element}
- 10/125 . . {the MOSFET being a thin film transistor [TFT]}
- 10/15 . {comprising a resistor load element}
- 10/18 . {Peripheral circuit regions}

##### **12/00 Dynamic random access memory [DRAM] devices**

- 12/01 . {Manufacture or treatment}
- 12/02 . . {for one transistor one-capacitor [1T-1C] memory cells}
- 12/03 . . . {Making the capacitor or connections thereto}
- 12/033 . . . . {the capacitor extending over the transistor}
- 12/0335 . . . . . {Making a connection between the transistor and the capacitor, e.g. plug}
- 12/036 . . . . {the capacitor extending under the transistor}
- 12/038 . . . . {the capacitor being in a trench in the substrate}
- 12/0383 . . . . . {wherein the transistor is vertical}
- 12/0385 . . . . . {Making a connection between the transistor and the capacitor, e.g. buried strap}
- 12/0387 . . . . . {Making the trench}
- 12/05 . . . {Making the transistor}
- 12/053 . . . . {the transistor being at least partially in a trench in the substrate (vertical transistor in combination with a capacitor formed in a substrate trench [H10B 12/0383](#))}
- 12/056 . . . . {the transistor being a FinFET}
- 12/09 . . {with simultaneous manufacture of the peripheral circuit region and memory cells}
- 12/10 . DRAM devices comprising bipolar components

##### **WARNING**

Group [H10B 12/10](#) is incomplete pending reclassification of documents from groups [H01L 27/1027](#), [H01L 27/1028](#) and [H10B 99/00](#).

All groups listed in this Warning should be considered in order to perform a complete search.

- 12/20 . {DRAM devices comprising floating-body transistors, e.g. floating-body cells}
- 12/30 . {DRAM devices comprising one-transistor - one-capacitor [1T-1C] memory cells}
- 12/31 . . {having a storage electrode stacked over the transistor}
- 12/312 . . . {with a bit line higher than the capacitor}
- 12/315 . . . {with the capacitor higher than a bit line}
- 12/318 . . . {the storage electrode having multiple segments}
- 12/33 . . {the capacitor extending under the transistor}
- 12/34 . . {the transistor being at least partially in a trench in the substrate}
- 12/36 . . {the transistor being a FinFET}
- 12/37 . . {the capacitor being at least partially in a trench in the substrate}
- 12/373 . . . {the capacitor extending under or around the transistor}
- 12/377 . . . {having a storage electrode extension located over the transistor}
- 12/39 . . {the capacitor and the transistor being in a same trench}
- 12/395 . . . {the transistor being vertical}
- 12/48 . . {Data lines or contacts therefor}
- 12/482 . . . {Bit lines}
- 12/485 . . . {Bit line contacts}
- 12/488 . . . {Word lines}
- 12/50 . {Peripheral circuit region structures}

##### Non-volatile memory devices

##### **20/00 Read-only memory [ROM] devices**

- 20/10 . ROM devices comprising bipolar components

##### **WARNING**

Group [H10B 20/10](#) is incomplete pending reclassification of documents from groups [H01L 27/1027](#), [H01L 27/1028](#) and [H10B 99/00](#).

All groups listed in this Warning should be considered in order to perform a complete search.

20/20	<ul style="list-style-type: none"> <li>• Programmable ROM [PROM] devices comprising field-effect components (<a href="#">H10B 20/10 takes precedence</a>)</li> </ul> <p><b>WARNING</b></p> <p>Group <a href="#">H10B 20/20</a> is impacted by reclassification into group <a href="#">H10B 20/25</a>.</p> <p>Groups <a href="#">H10B 20/20</a> and <a href="#">H10B 20/25</a> should be considered in order to perform a complete search.</p>	41/47	<ul style="list-style-type: none"> <li>• . . . with a floating-gate layer also being used as part of the peripheral transistor</li> </ul>
		41/48	<ul style="list-style-type: none"> <li>• . . . with a tunnel dielectric layer also being used as part of the peripheral transistor</li> </ul>
		41/49	<ul style="list-style-type: none"> <li>• . . comprising different types of peripheral transistor</li> </ul>
		41/50	<ul style="list-style-type: none"> <li>• characterised by the boundary region between the core region and the peripheral circuit region</li> </ul>
		41/60	<ul style="list-style-type: none"> <li>• the control gate being a doped region, e.g. single-poly memory cell</li> </ul>
20/25	<ul style="list-style-type: none"> <li>• . One-time programmable ROM [OTPROM] devices, e.g. using electrically-fusible links</li> </ul> <p><b>WARNING</b></p> <p>Group <a href="#">H10B 20/25</a> is incomplete pending reclassification of documents from group <a href="#">H10B 20/20</a>.</p> <p>Groups <a href="#">H10B 20/20</a> and <a href="#">H10B 20/25</a> should be considered in order to perform a complete search.</p>	41/70	<ul style="list-style-type: none"> <li>• the floating gate being an electrode shared by two or more components</li> </ul>
		<b>43/00</b>	<b>EEPROM devices comprising charge-trapping gate insulators</b>
		43/10	<ul style="list-style-type: none"> <li>• characterised by the top-view layout</li> </ul>
		43/20	<ul style="list-style-type: none"> <li>• characterised by three-dimensional arrangements, e.g. with cells on different height levels</li> </ul>
		43/23	<ul style="list-style-type: none"> <li>• . with source and drain on different levels, e.g. with sloping channels</li> </ul>
		43/27	<ul style="list-style-type: none"> <li>• . . the channels comprising vertical portions, e.g. U-shaped channels</li> </ul>
20/27	<ul style="list-style-type: none"> <li>• {ROM only}</li> </ul>	43/30	<ul style="list-style-type: none"> <li>• characterised by the memory core region</li> </ul>
20/30	<ul style="list-style-type: none"> <li>• . {having the source region and the drain region on the same level, e.g. lateral transistors}</li> </ul>	43/35	<ul style="list-style-type: none"> <li>• . with cell select transistors, e.g. NAND</li> </ul>
20/34	<ul style="list-style-type: none"> <li>• . . {Source electrode or drain electrode programmed}</li> </ul>	43/40	<ul style="list-style-type: none"> <li>• characterised by the peripheral circuit region</li> </ul>
20/36	<ul style="list-style-type: none"> <li>• . . {Gate programmed, e.g. different gate material or no gate}</li> </ul>	43/50	<ul style="list-style-type: none"> <li>• characterised by the boundary region between the core and peripheral circuit regions</li> </ul>
20/363	<ul style="list-style-type: none"> <li>• . . . {Gate conductor programmed}</li> </ul>	<b>51/00</b>	<b>Ferroelectric RAM [FeRAM] devices comprising ferroelectric memory transistors</b>
20/367	<ul style="list-style-type: none"> <li>• . . . {Gate dielectric programmed, e.g. different thickness}</li> </ul>	51/10	<ul style="list-style-type: none"> <li>• characterised by the top-view layout</li> </ul>
20/38	<ul style="list-style-type: none"> <li>• . . {Doping programmed, e.g. mask ROM}</li> </ul>	51/20	<ul style="list-style-type: none"> <li>• characterised by the three-dimensional arrangements, e.g. with cells on different height levels</li> </ul>
20/383	<ul style="list-style-type: none"> <li>• . . . {Channel doping programmed}</li> </ul>	51/30	<ul style="list-style-type: none"> <li>• characterised by the memory core region</li> </ul>
20/387	<ul style="list-style-type: none"> <li>• . . . {Source region or drain region doping programmed}</li> </ul>	51/40	<ul style="list-style-type: none"> <li>• characterised by the peripheral circuit region</li> </ul>
20/40	<ul style="list-style-type: none"> <li>• . {having the source region and drain region on different levels, e.g. vertical channel}</li> </ul>	51/50	<ul style="list-style-type: none"> <li>• characterised by the boundary region between the core and peripheral circuit regions</li> </ul>
20/50	<ul style="list-style-type: none"> <li>• . {having transistors on different levels, e.g. 3D ROM}</li> </ul>	<b>53/00</b>	<b>Ferroelectric RAM [FeRAM] devices comprising ferroelectric memory capacitors</b>
20/60	<ul style="list-style-type: none"> <li>• {Peripheral circuit regions}</li> </ul>	53/10	<ul style="list-style-type: none"> <li>• characterised by the top-view layout</li> </ul>
20/65	<ul style="list-style-type: none"> <li>• . {of memory structures of the ROM only type}</li> </ul>	53/20	<ul style="list-style-type: none"> <li>• characterised by the three-dimensional arrangements, e.g. with cells on different height levels</li> </ul>
<b>41/00</b>	<b>Electrically erasable-and-programmable ROM [EEPROM] devices comprising floating gates</b>	53/30	<ul style="list-style-type: none"> <li>• characterised by the memory core region</li> </ul>
41/10	<ul style="list-style-type: none"> <li>• characterised by the top-view layout</li> </ul>	53/40	<ul style="list-style-type: none"> <li>• characterised by the peripheral circuit region</li> </ul>
41/20	<ul style="list-style-type: none"> <li>• characterised by three-dimensional arrangements, e.g. with cells on different height levels</li> </ul>	53/50	<ul style="list-style-type: none"> <li>• characterised by the boundary region between the core and peripheral circuit regions</li> </ul>
41/23	<ul style="list-style-type: none"> <li>• . with source and drain on different levels, e.g. with sloping channels</li> </ul>	<b>61/00</b>	<b>Magnetic memory devices, e.g. magnetoresistive RAM [MRAM] devices</b>
41/27	<ul style="list-style-type: none"> <li>• . . the channels comprising vertical portions, e.g. U-shaped channels</li> </ul>		<b>WARNING</b>
41/30	<ul style="list-style-type: none"> <li>• characterised by the memory core region</li> </ul>		Group <a href="#">H10B 61/00</a> is incomplete pending reclassification of documents from group <a href="#">H10N 59/00</a> .
41/35	<ul style="list-style-type: none"> <li>• . with a cell select transistor, e.g. NAND</li> </ul>		Groups <a href="#">H10N 59/00</a> and <a href="#">H10B 61/00</a> should be considered in order to perform a complete search.
41/40	<ul style="list-style-type: none"> <li>• characterised by the peripheral circuit region</li> </ul>		
41/41	<ul style="list-style-type: none"> <li>• . of a memory region comprising a cell select transistor, e.g. NAND</li> </ul>	61/10	<ul style="list-style-type: none"> <li>• {comprising components having two electrodes, e.g. diodes or MIM elements}</li> </ul>
41/42	<ul style="list-style-type: none"> <li>• . Simultaneous manufacture of periphery and memory cells</li> </ul>	61/20	<ul style="list-style-type: none"> <li>• {comprising components having three or more electrodes, e.g. transistors}</li> </ul>
41/43	<ul style="list-style-type: none"> <li>• . . comprising only one type of peripheral transistor</li> </ul>	61/22	<ul style="list-style-type: none"> <li>• . {of the field-effect transistor [FET] type}</li> </ul>
41/44	<ul style="list-style-type: none"> <li>• . . . with a control gate layer also being used as part of the peripheral transistor</li> </ul>		
41/46	<ul style="list-style-type: none"> <li>• . . . with an inter-gate dielectric layer also being used as part of the peripheral transistor</li> </ul>		

63/00	<b>Resistance change memory devices, e.g. resistive RAM [ReRAM] devices</b> <b>WARNING</b> <p>Group <a href="#">H10B 63/00</a> is impacted by reclassification into groups <a href="#">H10B 63/10</a> and <a href="#">H10N 79/00</a>.</p> <p>All groups listed in this Warning should be considered in order to perform a complete search.</p>	99/00	<b>Subject matter not provided for in other groups of this subclass</b> <b>WARNING</b> <p>Group <a href="#">H10B 99/00</a> is incomplete pending reclassification of documents from groups <a href="#">H01L 27/102</a> and <a href="#">H01L 27/1022</a>.</p> <p>Group <a href="#">H10B 99/00</a> is also impacted by reclassification into groups <a href="#">H10B 10/10</a>, <a href="#">H10B 12/10</a> and <a href="#">H10B 20/10</a>.</p> <p>All groups listed in this Warning should be considered in order to perform a complete search.</p>
63/10	. Phase change RAM [PCRAM, PRAM] devices <b>WARNING</b> <p>Group <a href="#">H10B 63/10</a> is incomplete pending reclassification of documents from group <a href="#">H10B 63/00</a>.</p> <p>Groups <a href="#">H10B 63/00</a> and <a href="#">H10B 63/10</a> should be considered in order to perform a complete search.</p>		
63/20	. {comprising selection components having two electrodes, e.g. diodes} 		
63/22	. . {of the metal-insulator-metal type} 		
63/24	. . {of the Ovonic threshold switching type} 		
63/30	. {comprising selection components having three or more electrodes, e.g. transistors} 	99/14	. {Memory cells having a cross-point geometry} <b>WARNING</b> <p>Group <a href="#">H10B 99/14</a> is incomplete pending reclassification of documents from group <a href="#">H01L 27/10</a>.</p> <p>Groups <a href="#">H01L 27/10</a> and <a href="#">H10B 99/10</a> should be considered in order to perform a complete search.</p>
63/32	. . {of the bipolar type} 		
63/34	. . {of the vertical channel field-effect transistor type} 		
63/80	. {Arrangements comprising multiple bistable or multi-stable switching components of the same type on a plane parallel to the substrate, e.g. cross-point arrays} 		
63/82	. . {the switching components having a common active material layer} 		
63/84	. . {arranged in a direction perpendicular to the substrate, e.g. 3D cell arrays} 	99/16	. {comprising memory cells having diodes} <b>WARNING</b> <p>Group <a href="#">H10B 99/16</a> is incomplete pending reclassification of documents from group <a href="#">H01L 27/101</a>.</p> <p>Groups <a href="#">H01L 27/101</a> and <a href="#">H10B 99/14</a> should be considered in order to perform a complete search.</p>
63/845	. . . {the switching components being connected to a common vertical conductor} 		
69/00	<b>Erasable-and-programmable ROM [EPROM] devices not provided for in groups <a href="#">H10B 41/00</a> - <a href="#">H10B 63/00</a>, e.g. ultraviolet erasable-and-programmable ROM [UVEPROM] devices</b> <b>WARNING</b> <p>Group <a href="#">H10B 69/00</a> is incomplete pending reclassification of documents from groups <a href="#">H01L 27/1027</a> and <a href="#">H01L 27/1028</a>.</p> <p>Groups <a href="#">H01L 27/1027</a>, <a href="#">H01L 27/1028</a> and <a href="#">H10B 69/00</a> should be considered in order to perform a complete search.</p>		
80/00	<b>Assemblies of multiple devices comprising at least one memory device covered by this subclass</b> <b>WARNING</b> <p>Group <a href="#">H10B 80/00</a> is incomplete pending reclassification of documents from groups <a href="#">H01L 25/065</a>, <a href="#">H01L 25/0652</a>, <a href="#">H01L 25/0655</a>, <a href="#">H01L 25/0657</a> and <a href="#">H01L 25/18</a>.</p> <p>All groups listed in this Warning should be considered in order to perform a complete search.</p>	99/20	. {comprising memory cells having thyristors} <b>WARNING</b> <p>Group <a href="#">H10B 99/20</a> is incomplete pending reclassification of documents from groups <a href="#">H01L 27/1027</a> and <a href="#">H01L 27/1028</a>.</p> <p>Groups <a href="#">H01L 27/1027</a>, <a href="#">H01L 27/1028</a> and <a href="#">H10B 99/20</a> should be considered in order to perform a complete search.</p>
		99/22	. {including field-effect components} <b>WARNING</b> <p>Group <a href="#">H10B 99/22</a> is incomplete pending reclassification of documents from group <a href="#">H01L 27/105</a>.</p> <p>Groups <a href="#">H01L 27/105</a> and <a href="#">H10B 99/22</a> should be considered in order to perform a complete search.</p>