ECLA EUROPEAN CLASSIFICATION

G11C STATIC STORES (information storage based on relative movement between record carrier and transducer G11B; semiconductor devices for storage H01L, e.g. H01L27/108 to H01L27/115; pulse technique in general H03K, e.g. electronic switches H03K17/00; [N: using a static store as a picture recording medium H04N5/907])

[N: **WARNING**
[C2011.01]

1. The following IPC groups are not used in the internal ECLA classification scheme. Subject matter covered by these groups is classified in the following ECLA groups:

G11C8/02	covered by	G11C8/00, H03K17/00
G11C11/4193	covered by	G11C11/00
G11C11/4195	covered by	G11C11/00
G11C11/4197	covered by	G11C11/00

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Notes

1. This subclass covers devices or arrangements for storage of digital or analogue information in which no relative movement takes place between an information storage element and a transducer; which incorporate a selecting-device for writing-in or reading-out the information into or from the store

2. This subclass does not cover elements not adapted for storage and not provided with such means as referred to in Note (3) below, which elements are classified in the appropriate subclass, e.g. of H01, H03K.

3. In this subclass, the following terms are used with the meaning indicated:
- "storage element" is an element which can hold at least one item of information and is provided with means for writing-in or reading-out this information;
- "memory" is a device, including storage elements, which can hold information to be extracted when desired.

[N0908]

G11C5/00 **Details of stores covered by G11C11/00**

G11C5/00R . [N: Circuit means for protection against loss of information of semiconductor storage devices (manufacturing semi-conductor by using bombardement with radiation H01L21/26; error detection, monitoring G06F11/00)]

G11C5/02 . Disposition of storage elements, e.g. in the form of a matrix array

G11C5/02S . . [N: Geometric lay-out considerations of storage- and peripheral-blocks in a semiconductor storage device (geometrical lay-out of the components in integrated circuits, H01L27/02B2)]

G11C5/04 . . Supports for storage elements, Supports for storage elements, [N: e.g. memory modules]; Mounting or fixing of storage elements on such supports [M1112]

G11C5/05 . . . Supporting of cores in matrix

G11C5/06 . Arrangements for interconnecting storage elements electrically, e.g. by wiring

G11C5/06H . . [N: Voltage and signal distribution in integrated semi-conductor memory access lines, e.g. word-line, bit-line, cross-over resistance, propagation delay]

G11C5/06M . . [N: Means for reducing external access-lines for a semiconductor memory clip e.g. by multiplexing at least address and data signals]

G11C5/08 . . for interconnecting magnetic elements, e.g. toroidal cores

G11C5/10 . . for interconnecting capacitors

G11C5/12 . Apparatus or processes for interconnecting storage elements, e.g. for threading magnetic cores

G11C5/14 . Power supply arrangements (in general G05F, H02J, H02M), [N: e.g. Power down/chip (de)selection, layout of wiring/power grids, multiple supply levels]

G11C5/14B . . [N: Battery and back-up supplies (back-up supplies per se H02J9/06B)]

G11C5/14C . . [N: Contactless power supplies, e.g. RF, induction, IR (in general H02J5/00)]

G11C5/14D . . [N: Detection of memory cassette insertion/removal; Continuity checks of supply and ground lines (in general G01R31/02); Detection of supply variations/interruptions/levels (G11C5/14S takes precedence); Switching between alternative supplies (back-up supplies per se H02J9/06B), (G11C5/14B takes precedence)] [C1112]

G11C5/14D1 . . . [N: Detection of predetermined disconnection or reduction of power supply, e.g. power down or power standby] [N1112]

G11C5/14P . . [N: Applications of charge pumps (charge pumps per se H02M3/07); Boosted voltage circuits (for logic circuits or inverting circuits H03K19/00); Clamp circuits therefor (G11C5/14B takes precedence)]

G11C5/14P1 . . . [N: Substrate bias generators (G11C5/14B takes precedence; in general G05F3/20S)]

G11C5/14R . . [N: Voltage reference generators, voltage and current regulators (in general G05F3/24); Internally lowered supply level (in general G05F1/46B); Compensation for voltage drops (G11C5/14B takes precedence)]

G11C5/14S . . [N: Details of power up or power down circuits, standby circuits or recovery circuits] [N1112]

G11C7/00 **Arrangements for writing information into, or reading information out from, a digital store** (G11C5/00 takes precedence; auxiliary circuits for stores using semiconductor devices G11C11/4063, G11C11/413, G11C11/4193) [C0105]

G11C7/00R . [N: with combined beam-and individual cell access]

G11C7/02 . with means for avoiding parasitic signals [N0506]

[N: **WARNING**
Not complete; see also G11C7/18, G11C7/22
]

G11C7/04 . with means for avoiding disturbances due to temperature effects [N0506]

[N: **WARNING**
Not complete; see also G11C7/22
]

G11C7/06 . Sense amplifiers; Associated circuits, [N: e.g. timing or triggering circuits] (amplifiers per se H03F, H03K) [C9804]

G11C7/06C . . [N: Differential amplifiers of non-latching type, e.g. comparators, long-tailed pairs] [N9804]

G11C7/06L . . [N: Differential amplifiers of latching type] [N9804]

G11C7/06S . . [N: Single-ended amplifiers] [N9804]

G11C7/08 . . Control thereof [N0506]

[N: **WARNING**
Not complete; see also G11C7/06
]

G11C7/10 . Input/output (I/0) data interface arrangements, e.g. I/0 data control circuits, I/O data buffers (level conversion circuits in general H03K19/0175) [N9802]

G11C7/10D . . [N: Interface circuits for daisy chain or ring bus memory arrangements] [N1205]

G11C7/10L . . [N: Data managing, e.g. manipulating data before writing or reading out, data bus switches or control circuits therefor] [N9802]

G11C7/10L1 . . . [N: Data masking during input/output] [N1205]

G11C7/10L3 . . . [N: Data reordering during input/output, e.g. crossbars, layers of multiplexers, shifting or rotating] [N1205]

G11C7/10M . . [N: Read-write modes for single port memories, i.e. having either a random port or a serial port] [N9802]

G11C7/10M2 . . . [N: Serial bit line access mode, e.g. using bit line address shift registers, bit line address counters, bit line burst counters] [N9802]

G11C7/10M2A . . . . [N: Page serial bit line access mode, i.e. using an enabled row address stroke pulse with its associated word line address and a sequence of enabled column address stroke pulses each with its associated bit line address] [N9802]

G11C7/10M2A2 . . . . . [N: Extended data output (EDO) mode, i.e. keeping output buffer enabled during an extended period of time] [N9802]

G11C7/10M2B . . . . [N: Static column decode serial bit line access mode, i.e. using an enabled row address stroke pulse with its associated word line address and a sequence of enabled bit line addresses] [N9802]

G11C7/10M3 . . . [N: using serially addressed read-write data registers (G11C7/10M4 takes precedence)] [N9802]

G11C7/10M3A . . . . [N: using data registers of which only one stage is addressed for sequentially outputting data from a predetermined number of stages, e.g. nibble read-write mode] [N9802]

G11C7/10M4 . . . [N: using data shift registers] [N9802]

G11C7/10M5 . . . [N: using pipelining techniques, i.e. using latches between functional memory parts, e.g. row/column decoders, I/O buffers, sense amplifiers] [N9802]

G11C7/10M6 . . . [N: using interleaving techniques, i.e. read-write of one part of the memory while preparing another part] [N9802]

G11C7/10M7 . . . [N: Read-write mode select circuits] [N9802]

G11C7/10P . . [N: Data bus control circuits, e.g. precharging, presetting, equalising] [N9802]

G11C7/10R . . [N: Data output circuits, e.g. read-out amplifiers, data output buffers, data output registers, data output level conversion circuits] [N9802]

G11C7/10R1 . . . [N: Optical output buffers] [N1205]

G11C7/10R2 . . . [N: Data output buffers, e.g. comprising level conversion circuits, circuits for adapting load] [N1205]

G11C7/10R3 . . . [N: Data output latches] [N1205]

G11C7/10R5 . . . [N: Control signal output circuits, e.g. status or busy flags, feedback command signals] [N1205]

G11C7/10R7 . . . [N: Output synchronization] [N1205]

G11C7/10R9 . . . [N: I/O lines read out arrangements (global or local sense amplifiers for bit lines G11C7/06)] [N1205]

G11C7/10S . . [N: for memories with random access ports synchronised on clock signal pulse trains, e.g. synchronous memories, self timed memories] [N9802]

G11C7/10T . . [N: for multiport memories each having random access ports and serial ports, e.g. video RAM] [N9802]

G11C7/10W . . [N: Data input circuits, e.g. write amplifiers, data input buffers, data input registers, data input level conversion circuits] [N9802]

G11C7/10W1 . . . [N: Optical input buffers] [N1205]

G11C7/10W2 . . . [N: Data input buffers, e.g. comprising level conversion circuits, circuits for adapting load] [N1205]

G11C7/10W3 . . . [N: Data input latches] [N1205]

G11C7/10W5 . . . [N: Control signal input circuits] [N1205]

G11C7/10W7 . . . [N: Input synchronization] [N1205]

G11C7/10W9 . . . [N: Write circuits, e.g. I/O line write drivers] [N1205]

G11C7/12 . Bit line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, equalising circuits, for bit lines [N9802]

G11C7/14 . Dummy cell management; Sense reference voltage generators [N9802]

G11C7/16 . Storage of analogue signals in digital stores using an arrangement comprising analogue/digital (A/D) converters, digital memories and digital/analogue (D/A) converters [N9802]

G11C7/18 . Bit line organisation; Bit line lay-out [N9802]

G11C7/20 . Memory initialisation circuits, e.g. when powering up or down, memory clear, latent image memory [N9802]

G11C7/22 . Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators or management [N9802]

G11C7/22A . . [N: Clock generating, synchronizing or distributing circuits within memory device] [N1205]

G11C7/22B . . [N: Clock input buffers] [N1205]

G11C7/22D . . [N: Timing of memory operations based on dummy memory elements or replica circuits] [N1205]

G11C7/24 . Memory cell safety or protection circuits, e.g. arrangements for preventing inadvertent reading or writing; Status cells; Test cells [N9802]

G11C8/00 **Arrangements for selecting an address in a digital store (for stores using transistors G11C11/407, G11C11/413; [N: switching or gating circuits for general use H03K17/00])** [C0607]

G11C8/00W . [N: with travelling wave access]

G11C8/04 . using a sequential addressing device, e.g. shift register, counter [N: (FIFO G06F5/06;

LIFO G06F7/78; multidimensional memory addressing G06F12/02B)]

G11C8/06 . Address interface arrangements, e.g. address buffers (level conversion circuits in general H03K19/0175) [N0111]

G11C8/08 . Word line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, for word lines [N0111]

G11C8/10 . Decoders [N0111]

G11C8/12 . Group selection circuits, e.g. for memory block selections, chip selection, array selection [N0111]

G11C8/14 . Word line organisation; Word line lay-out [N0111]

G11C8/16 . Multiple access memory array, e.g. addressing one storage element via at least independent addressing line groups [N: (multiport memories in general G11C7/10T)] [N0111] [M1112]

G11C8/18 . Address timing or clocking circuits; Address control signal generation or management, e.g. for row address strobe (RAS) or column address strobe (CAS) signals [N0111]

G11C8/20 . Address safety or protection circuits, i.e. arrangements for preventing unauthorised or accidental access [N0111]

G11C11/00 **Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor** (G11C14/00 to G11C21/00 take precedence)

G11C11/00C . [N: comprising combined but independently operative RAM-ROM, RAM-PROM, RAM-EPROM cells]

Note
Group G11C11/56 takes precedence over groups G11C11/02 to G11C11/54

G11C11/02 . using magnetic elements [N: (using multibit magnetic storage elements G11C11/56B; counters with magnetic elements H03K23/76; pulse generators, static switches, logic circuits with such elements H03K3/45, H03K17/80, H03K19/16; measurement of magnetic variables G01R33/00)] [C0210]

G11C11/04 . . using rod-type storage elements [N: contains no documents; see G11C11/06C, G11C11/14, G11C11/155]

G11C11/06 . . using single-aperture storage elements, e.g. ring core; using multi-aperture plates in which each individual aperture forms a storage element

G11C11/06B . . . [N: using a single aperture or single magnetic closed circuit]

[N: **Note**
Provisionally contains the following details; control write -, read -, address circuitry (pulse generators in general H03K5/00, H03K17/00); arrangements for temperature compensation; checking of the correct functioning and repair arrangements (checking methods in general G06F11/00, G06F11/28; testing magnetic elements per se G01R33/00); magnetic properties, choice of materials or the like (materials per se H01F1/00)
]

G11C11/06B1 . . . . [N: using one such element pro bit]

G11C11/06B1B . . . . . [N: with destructive read-out]

G11C11/06B1B2 . . . . . [N: Matrixes]

G11C11/06B1B2B . . . . . {7 dots} [N: "bit"- organised, e.g. 2 1/2D, 3D or a similar organisation, i.e. bit core selection for writing or reading, by at least two coincident partial currents]

G11C11/06B1B2C . . . . . {7 dots} [N: "word"-organised, e.g. 2D organisation or linear selection, i.e. full current selection through all the bit-cores of a word during reading]

G11C11/06B1C . . . . . [N: with non-destructive read-out]

G11C11/06B1C2 . . . . . [N: Matrixes]

G11C11/06B1C2B . . . . . {7 dots} [N: "bit"-organised (2 1/2D, 3D or similar organisation)]

G11C11/06B1C2C . . . . . {7 dots} [N: "word"-organised (2D organisation or linear selection)]

G11C11/06B2 . . . . [N: using two or more such elements pro bit]

G11C11/06C . . . [N: Multi-aperture structures or multi-magnetic closed circuits, each aperture storing a "bit", realised by rods, plates, grids, waffle-irons, (i.e. grooved plates) or similar devices]

G11C11/06D . . . [N: Multi-aperture structures or multi-magnetic closed circuits using two or more apertures per bit]

G11C11/061 . . . using element with single aperture or magnetic loop for storage, one element per bit, and for destructive read-out [N: contains no documents, see G11C11/06B, G11C11/06B1, G11C11/06B1B, G11C11/06B1B2]

G11C11/063 . . . . bit organised, such as 2 1/2D, 3D organisation, i.e. for selection of an element by means of at least two coincident parital currents both for reading and for writing [N: contains no documents; see G11C11/06B1B2B]

G11C11/065 . . . . word organised, such as 2D organisation, or linear selection, i.e. for selection of all the elements of a word by means of a single full current for reading [N: contains no documents; see G11C11/06B1B2C]

G11C11/067 . . . using elements with single aperture or magnetic loop for storage, one element per bit, and for non-destructive read-out [N: contains no documents, see G11C11/06B1C to G11C11/06B1C2C]

G11C11/08 . . using multi-aperture storage elements, e.g. using transfluxors; using plates incorporating several individual multi-aperture storage elements (G11C11/10 takes precedence; using multi-aperture plates in which each individual aperture forms a storage element G11C11/06)

G11C11/10 . . using multi-axial storage elements

G11C11/12 . . using tensors; using twistors, i.e. elements in which one axis of magnetisation is twisted

G11C11/14 . . using thin-film elements

G11C11/15 . . . using multiple magnetic layers (G11C11/155 takes precedence)

G11C11/155 . . . with cylindrical configuration

G11C11/16 . . using elements in which the storage effect is based on magnetic spin effect [N: (sensors using magnetoresistive multilayer structures G01R33/09B; thin layer magnetic read heads for magnetic discs G11B5/31; non-reciprocal magnetic elements in waveguides H01P; composition of ferromagnetic material H01F1/00; gyrators H03H7/00B)] [M1206]

G11C11/161 . . . [N: details concerning the memory cell structure, e.g. the layers of the ferromagnetic memory cell] [N1205]

G11C11/165 . . . [N: Auxiliary circuits] [N1205]

G11C11/1653 . . . . [N: Address circuits or decoders] [N1205]

G11C11/1655 . . . . . [N: Bit-line or column circuits] [N1205]
G11C11/1657 . . . . . [N: Word-line or row circuits] [N1205]
G11C11/1659 . . . . [N: Cell access] [N1205]
G11C11/1673 . . . . [N: Reading or sensing circuits or methods] [N1205]
G11C11/1675 . . . . [N: Writing or programming circuits or methods] [N1205]
G11C11/1677 . . . . [N: Verifying circuits or methods] [N1205]
G11C11/1693 . . . . [N: Timing circuits or methods] [N1205]
G11C11/1695 . . . . [N: Protection circuits or methods] [N1205]
G11C11/1697 . . . . [N: Power supply circuits] [N1205]

G11C11/18 . using Hall-effect devices

G11C11/19 . using non-linear reactive devices in resonant circuits [N: contains no documents, see G11C11/20]
G11C11/20 . . using parametrons, [N: i.e. ferroresonant triggers; with overcritica feedback magnetic amplifiers or similar (pulse generators using parametrons and ferroresonant devices H03K19/162, H03K19/164; counters using such elements H03K23/00B)]

G11C11/21 . using electric elements
G11C11/22 . . using ferroelectric elements [N: (using multibit ferroelectric storage elements G11C11/56F; pulse generators using ferroelectric elements H03K3/45; counters using such elements H03K23/76)] [C0210]
G11C11/221 . . . [N: using ferroelectric capacitors] [N1205]
G11C11/223 . . . [N: using MOS with ferroelectric gate insulating film] [N1205]
G11C11/225 . . . [N: Auxiliary circuits] [N1205]
G11C11/2253 . . . . [N: Address circuits or decoders] [N1205]
G11C11/2255 . . . . . [N: Bit-line or column circuits] [N1205]
G11C11/2257 . . . . . [N: Word-line or row circuits] [N1205]
G11C11/2259 . . . . [N: Cell access] [N1205]
G11C11/2273 . . . . [N: Reading or sensing circuits or methods] [N1205]
G11C11/2275 . . . . [N: Writing or programming circuits or methods] [N1205]
G11C11/2277 . . . . [N: Verifying circuits or methods] [N1205]
G11C11/2293 . . . . [N: Timing circuits or methods] [N1205]
G11C11/2295 . . . . [N: Protection circuits or methods] [N1205]
G11C11/2297 . . . . [N: Power supply circuits] [N1205]
G11C11/23 . . using electrostatic storage on a common layer, e.g. Forrester-Haef tubes, [N: William tubes] (G11C11/22 takes precedence; [N: construction of Williams tubes H01J31/00]) [C9807]
G11C11/24 . . using capacitors (G11C11/22 takes precedence; using a combination of semiconductor devices and capacitors G11C11/34, e.g. G11C11/40)
G11C11/26 . . using discharge tubes [N: (counters using such elements H03K25/00)]
G11C11/26B . . . [N: counting tubes, e.g. decatrons, trochotrons (counters using such elements H03K29/00)] [C9807]
G11C11/28 . . . using gas-filled tubes [N: counting tubes G11C11/26B; pulse generators, electronic switches, logic circuits using such elements H03K3/37, H03K17/52, H03K19/04]

G11C11/30 . . . using vacuum tubes [N: counting tubes G11C11/26B; pulse generators, electronic switches, logic circuits using such elements H03K3/37, H03K17/52, H03K19/04]

G11C11/34 . . using semiconductor devices [N: (processes or apparatus for the manufacture or treatment of semiconductor or solid state devices H01L21/00; integrated circuit devices H01L27/00; generating electric pulses, e.g. bistable devices using semiconductor devices H03K3/00)] [C9807]

G11C11/35 . . . with charge storage in a depletion layer, e.g. charged coupled devices [N: (in shift registers G11C19/28B)] [N0506]

G11C11/36 . . . using diodes, e.g. as threshold elements, [N: i.e. diodes assuming a stable ON-stage when driven above their threshold (S- or N-characteristic)]

G11C11/38 . . . . using tunnel diodes

G11C11/39 . . . using thyristors [N: or the avalanche or negative resistance type, e.g. PNPN, SCR, SCS, UJT]

G11C11/40 . . . using transistors [C0105]

G11C11/401 . . . . forming cells needing refreshing or charge regeneration, [N: i.e. dynamic cells]

G11C11/402 . . . . . with charge regeneration individual to each memory cell, i.e. internal refresh

G11C11/402A . . . . . [N: using field effect transistors]

G11C11/402B . . . . . [N: using bipolar transistors]

G11C11/403 . . . . . with charge regeneration common to a multiplicity of memory cells, i.e. external refresh

G11C11/404 . . . . . with one charge-transfer gate, e.g. MOS transistor, per cell

G11C11/404N . . . . . {7 dots} [N: using a plurality of serially connected access transistors, each having a storage capacitor] [N9810]

[N: **WARNING**
Not complete, see also G11C11/404
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G11C11/405 . . . . . with three charge-transfer gates, e.g. MOS transistors, per cell

G11C11/406 . . . . . Management or control of the refreshing or charge-regeneration cycles

G11C11/406A . . . . . [N: Arbitration, priority and concurrent access to memory cells for read/write or refresh operations] [N1205]

G11C11/406C . . . . . [N: Refresh operations in memory devices with an internal cache or data buffer] [N1205]

G11C11/406E . . . . . [N: External triggering or timing of internal or partially internal refresh operations, e.g. auto-refresh or CAS-before-RAS triggered refresh] [N1205]

G11C11/406I . . . . . [N: Internal triggering or timing of refresh, e.g. hidden refresh, self refresh, pseudo-SRAMs] [N1205]

G11C11/406M . . . . . [N: Refresh operations over multiple banks or interleaving] [N1205]

G11C11/406P . . . . . [N: Partial refresh of memory arrays] [N1205]

G11C11/406T . . . . . [N: Temperature related aspects of refresh operations] [N1205]

G11C11/4063 . . . . . Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing or timing [N0105]

G11C11/4067 . . . . . for memory cells of the bipolar type [N0105]

G11C11/407 . . . . . for memory cells of the field-effect type [C0105]

G11C11/4072 . . . . . {7 dots} Circuits or initialisation, powering up or down, clearing

memory or presetting [N0105]

G11C11/4074 . . . . . {7 dots} Power supply or voltage generation circuits, e.g. bias voltage generators, substrate voltage generators, back-up power, power control circuits [N0105]

G11C11/4076 . . . . . {7 dots} Timing circuits (for regeneration management G11C11/406) [N0105]

G11C11/4078 . . . . . {7 dots} Safety or protection circuits, e.g. for preventing inadvertent or unauthorised reading or writing; Status cells; Test cells (protection of memory contents during checking or testing G11C29/52) [N0105] [C0505]

G11C11/408 . . . . . {7 dots} Address circuits [C0105]

G11C11/408B . . . . . {8 dots} [N: Address Buffers; level conversion circuits]

G11C11/408C . . . . . {8 dots} [N: Word line control circuits, e.g. word line drivers, - boosters, - pull-up, - pull-down, - precharge]

G11C11/408D . . . . . {8 dots} [N: Address decoders, e.g. bit - or word line decoders; Multiple line decoders]

G11C11/409 . . . . . {7 dots} Read-write (R-W) circuits [C0105]

G11C11/4091 . . . . . {8 dots} Sense or sense/refresh amplifiers, or associated sense circuitry, e.g. for coupled bit-line precharging, equalising or isolating [N0105]

G11C11/4093 . . . . . {8 dots} Input/output (I/O) data interface arrangements, e.g. data buffers (level conversion circuits in general H03K19/0175) [N0105]

G11C11/4094 . . . . . {8 dots} Bit-line management or control circuits [N0105]

G11C11/4096 . . . . . {8 dots} Input/output (I/O) data management or control circuits, e.g. reading or writing circuits, I/O drivers, bit-line switches [N0105]

G11C11/4097 . . . . . {8 dots} Bit-line organisation, e.g. bit-line layout, folded bit lines [N0105]

G11C11/4099 . . . . . {8 dots} Dummy cell treatment; Reference voltage generators [N0105]

G11C11/41 . . . . forming [N: static] cells with positive feedback, i.e. cells not needing refreshing or charge regeneration, e.g. bistable multivibrator or Schmitt trigger

G11C11/411 . . . . . using bipolar transistors only

G11C11/411B . . . . . [N: with at least one cell access to base or collector of at least one of said transistors, e.g. via access diodes, access transistors]

G11C11/411E . . . . . [N: with at least one cell access via separately connected emittors of said transistors or via multiple emittors, e.g. T2L, ECL]

G11C11/412 . . . . . using field-effect transistors only [N: (latent image memory G11C7/20; multi-port cells G11C8/160)] [C9807] [M1207]

G11C11/412R . . . . . [N: Cells incorporating circuit means for protection against loss of information (in general G11C5/00R)] [N9408]

G11C11/413 . . . . . Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing, timing, power reduction (in general G11C5/00 to G11C8/00)

G11C11/414 . . . . . for memory cells of the bipolar type

G11C11/415 . . . . . {7 dots} Address circuits

G11C11/416 . . . . . {7 dots} Read-write circuits

G11C11/417 . . . . . for memory cells of the field-effect type

G11C11/418 . . . . . {7 dots} Address circuits

G11C11/419 . . . . . {7 dots} Read-write circuits

G11C11/42 . . using opto-electronic devices, i.e. light-emitting and photoelectric devices electrically - or optically - [N: feedback -] coupled

G11C11/44 . . using super-conductive elements, e.g. cryotron [N: (pulse generators using such elements H03K3/38; counters H03K23/00B)]

G11C11/46 . using thermoplastic elements

G11C11/48 . using displaceable coupling elements, e.g. ferromagnetic cores, to produce change between different states of mutual or self-inductance [N: contains no documents; see G11C17/00 and subgroups]

G11C11/50 . using actuation of electric contacts to store the information (mechanical stores G11C23/00; switches provising a selected number of consecutive operations of the contacts by a single manual actuation of the operating part H01H41/00)

G11C11/52 . . using electromagnetic relays

G11C11/54 . using elements simulating biological cells, e.g. neuron

G11C11/56 . using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency (counting arrangements comprising multi-stable elements of this type H03K25/00, H03K29/00) [C1107]

G11C11/56B . . [N: using magnetic storage elements] [C0210]

G11C11/56C . . [N: using conductive bridging RAM [CBRAM] or programming metallization cells [PMC] [N1107]

G11C11/56D . . [N: using charge storage in a floating gate] [C0210]

G11C11/56D2 . . . [N: Programming or writing circuits; Data input circuits] [N0210]

G11C11/56D2E . . . . [N: Erasing circuits] [N0210]

G11C11/56D4 . . . [N: Sensing or reading circuits; Data output circuits] [N0210]

G11C11/56E . . [N: using capacitive charge storage elements] [C0210]

G11C11/56F . . [N: using ferroelectric storage elements] [N0210]

G11C11/56G . . [N: using organic memory material storage elements] [N1107]

G11C11/56M . . [N: using charge trapping in an insulator] [N0210]

G11C11/56P . . [N: using amorphous/crystalline phase transition storage elements] [N1107]

G11C11/56Q . . [N: using storage elements comprising metal oxide memory material, e.g. perovskites] [N1107]

G11C11/56R . . [N: read-only digital stores using storage elements with more than two stable states] [N0210] [C1107]

G11C13/00 **Digital stores characterised by the use of storage elements not covered by groups G11C11/00, G11C23/00 to G11C25/00**

G11C13/00R . [N: using resistance random access memory [RRAM] elements] [N1101] [C1107]

G11C13/00R1 . . [N: comprising amorphous/crystalline phase transition cells] [N1101]

G11C13/00R3 . . [N: comprising metal oxide memory material, e.g. perovskites] [N1101]

G11C13/00R5 . . [N: RRAM elements whose operation depends upon chemical change] [N1107]

G11C13/00R5B . . . [N: comprising conductive bridging RAM [CBRAM] or programming metallization

cells [PMCs]] [N1107]

G11C13/00R5C . . . [N: comprising cells based on organic memory material] [N1107]

G11C13/00R5C2 . . . . [N: comprising polymers] [N1107]

G11C13/00R5C4 . . . . [N: comprising bio-molecules] [N1107]

G11C13/00R25 . . [N: Auxiliary circuits] [N1101]

G11C13/00R25A . . . [N: Address circuits or decoders] [N1101]

G11C13/00R25A2 . . . . [N: Bit-line or column circuits] [N1101]

G11C13/00R25A4 . . . . [N: Word-line or row circuits] [N1101]

G11C13/00R25C . . . [N: Cell access] [N1101]

G11C13/00R25D . . . [N: Disturbance prevention or evaluation; Refreshing of disturbed memory data] [N1205]

G11C13/00R25E . . . [N: Evaluating degradation, retention or wearout, e.g. by counting writing cycles] [N1205]

G11C13/00R25P . . . [N: Power supply circuits] [N1101]

G11C13/00R25R . . . [N: Reading or sensing circuits or methods] [N1101]

G11C13/00R25S . . . [N: Security or protection circuits or methods] [N1107]

G11C13/00R25T . . . [N: Timing circuits or methods] [N1101]

G11C13/00R25V . . . [N: Verifying circuits or methods] [N1205]

G11C13/00R25W . . . [N: Writing or programming circuits or methods] [N1101]

G11C13/00R25Z . . . [N: Erasing, e.g. resetting, circuits or methods] [N1205]

G11C13/02 . using elements whose operation depends upon chemical change [N: (G11C13/00R5 takes precedence)]; using electrochemical charge G11C11/00) [C1107]

G11C13/02N . . [N: using fullerenes, e.g. C60, or nanotubes, e.g. carbon or silicon nanotubes] [N0508]

G11C13/04 . using optical elements [N: using other beam accessed elements, e.g. electron, ion beam (using electrostatic memory tubes G11C11/23; recording of television signals H04N5/76)] [C9807]

G11C13/04B . . [N: using photochromic storage elements (G11C13/04C takes precedence)]

G11C13/04C . . [N: using information stored in the form of an interference pattern (hologram, lippman; holography G03H, G02B5/32)]

G11C13/04C2 . . . [N: using magnetic-optical storage elements]

G11C13/04C4 . . . [N: using electro-optical elements]

G11C13/04C6 . . . [N: using photochromic storage elements]

G11C13/04C8 . . . [N: using other storage elements storing information in the form of an interference pattern] [C1101]

G11C13/04E . . [N: using electro-optical elements (G11C13/04C takes precedence)] [N9803]

G11C13/04F . . [N: using other optical storage elements] [C1101]

G11C13/06 . . using magneto-optical elements (magneto-optics in general G02F) [N: G11C13/04C takes precedence]

G11C14/00 **Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down** [N: bistable elements storing the actual state when the supply voltage fails H03K3/0233D, H03K3/037C, H03K3/286B, H03K3/356C] [C9508]

G11C14/00D . [N: in which the volatile element is a DRAM cell] [N1111]
G11C14/00D2 . . [N: and the nonvolatile element is an EEPROM element, e.g. a floating gate or MNOS transistor] [N1111]
G11C14/00D4 . . [N: and the nonvolatile element is a ferroelectric element] [N1111]
G11C14/00D6 . . [N: and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell] [N1111]
G11C14/00D8 . . [N: and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material.] [N1111]

G11C14/00F . [N: in which the volatile element is a SRAM cell] [N1111]
G11C14/00F2 . . [N: and the nonvolatile element is an EEPROM element, e.g. a floating gate or MNOS transistor] [N1111]
G11C14/00F4 . . [N: and the nonvolatile element is a ferroelectric element] [N1111]
G11C14/00F6 . . [N: and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell] [N1111]
G11C14/00F8 . . [N: and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material.] [N1111]

G11C15/00 **Digital stores in which information comprising one or more characteristic parts is written into the store and in which information is read-out by searching for one or more of these characteristic parts, i.e. associative or content-addressed stores** (in which information is addressed to a specific location G11C11/00; [N: selection information using addressing means, e.g. hashing, tree addressing, chaining, G06F11/22; information retrieval systems using a computer G06F17/30])

G11C15/02 . using magnetic elements

G11C15/04 . using semiconductor elements [C9508]
G11C15/04D . . [N: using capacitive charge storage elements] [N0210]
G11C15/04N . . [N: using non-volatile storage elements] [N9508]

G11C15/06 . using cryogenic elements

G11C16/00 **Erasable programmable read-only memories** (G11C14/00 takes precedence)

G11C16/02 . electrically programmable [N: (programmable multibit digital storage elements G11C11/56D)] [C0210]
G11C16/04 . . using variable threshold transistors, e.g. FAMOS [C9408]
G11C16/04F . . . [N: comprising cells containing floating gate transistors (G11C16/04N, G11C16/04V take precedence)] [N9408]
G11C16/04F1 . . . . [N: comprising cells containing a single floating gate transistor and no select transistor, e.g. UV EPROM] [N9408]
G11C16/04F2 . . . . [N. comprising cells containing a merged floating gate and select transistor] [N9408]
G11C16/04F3 . . . . [N: comprising cells containing a single floating gate transistor and one or more separate select transistors] [N9408]
G11C16/04F4 . . . . [N: comprising cells containing multiple floating gate devices, e.g. separate read-and-write FAMOS transistors with connected floating gates] [N9408]

G11C16/04F4C . . . . . [N: Floating gate memory cells with both P and N channel memory transistors, usually sharing a common floating gate] [N1203]

G11C16/04F4P . . . . . [N: comprising plural independent floating gates which store independent data (for storage of more than two stable states at a single floating gate G11C11/56D)] [N0211]

G11C16/04M . . . [N: comprising cells with charge storage in an insulating layer, e.g. MNOS, SNOS (G11C16/04N, G11C16/04V take precedence)] [N9408]

G11C16/04M2 . . . . . [N: comprising plural independent storage sites which store independent data (for storage of more than two stable states at a single storage site G11C11/56D)] [N0211]

G11C16/04N . . . [N: comprising cells having several storage transistors connected in series] [N9408]

G11C16/04V . . . [N: Virtual ground arrays] [N9408]

G11C16/06 . . Auxiliary circuits, e.g. for writing into memory (in general G11C7/00)

G11C16/08 . . . Address circuits; Decoders; Word-line control circuits [N9907]

G11C16/10 . . . Programming or data input circuits [N9907]

G11C16/10E . . . . [N: External programming circuits, e.g. EPROM programmers; In-circuit programming or reprogramming; EPROM emulators] [N9907]

G11C16/10E2 . . . . . [N: Circuits or methods for updating contents of nonvolatile memory, especially with 'security' features to ensure reliable replacement, i.e. preventing that old data is lost before new data is reliably written] [N1203]

G11C16/10P . . . . [N: Programming all cells in an array, sector or block to the same state prior to flash erasing] [N1203]

G11C16/12 . . . . Programming voltage switching circuits [N9907]

G11C16/14 . . . . Circuits for erasing electrically, e.g. erase voltage switching circuits [N9907]

G11C16/16 . . . . . for erasing blocks, e.g. arrays, words, groups [N9907]

G11C16/18 . . . . Circuits for erasing optically [N9907]

G11C16/20 . . . . Initialising; Data preset; Chip identification [N9907]

G11C16/22 . . . Safety or protection circuits preventing unauthorised or accidental access to memory cells [N9907]

G11C16/22V . . . . [N: Preventing erasure, programming or reading when power supply voltages are outside the required ranges] [N0107]

G11C16/24 . . . Bit-line control circuits [N9907]

G11C16/26 . . . Sensing or reading circuits; Data output circuits [N9907]

G11C16/28 . . . . using differential sensing or reference cells, e.g. dummy cells [N9907]

G11C16/30 . . . Power supply circuits [N9907]

G11C16/32 . . . Timing circuits [N9907]

G11C16/34 . . . Determination of programming status, e.g. threshold voltage, overprogramming or underprogramming, retention [N9907]

G11C16/34C . . . . [N: Convergence or correction of memory cell threshold voltages; Repair or recovery of overerased or overprogrammed cells] [N0107]

G11C16/34C2 . . . . . [N: Circuits or methods to recover overerased nonvolatile memory cells detected during erase verification, usually by means of a "soft" programming step] [N1203]

G11C16/34C4 . . . . . [N: Circuits or methods to recover overprogrammed nonvolatile memory cells detected during program verification, usually by means of a "soft" erasing step] [N1203]

G11C16/34D . . . . [N: Disturbance prevention or evaluation; Refreshing of disturbed memory

data] [N0107]

G11C16/34D2 . . . . . [N: Circuits or methods to evaluate read or write disturbance in nonvolatile memory, without steps to mitigate the problem] [N1203]

G11C16/34D4 . . . . . [N: Circuits or methods to prevent or reduce disturbance of the state of a memory cell when neighbouring cells are read or written] [N1203]

G11C16/34D6 . . . . . [N: Circuits or methods to detect disturbed nonvolatile memory cells, e.g. which still read as programmed but with threshold less than the program verify threshold or read as erased but with threshold greater than the erase verify threshold, and to reverse the disturbance via a refreshing programming or erasing step] [N1203]

G11C16/34V . . . . [N: Arrangements for verifying correct programming or erasure] [N0107]

G11C16/34V2 . . . . . [N: Arrangements for verifying correct erasure or for detecting overerased cells] [N0107]

G11C16/34V2C . . . . . [N: Circuits or methods to verify correct erasure of nonvolatile memory cells] [N1203]

G11C16/34V2D . . . . . [N: Circuits or methods to detect overerased nonvolatile memory cells, usually during erasure verification] [N1203]

G11C16/34V4 . . . . . [N: Arrangements for verifying correct programming or for detecting overprogrammed cells] [N0107]

G11C16/34V4C . . . . . [N: Circuits or methods to verify correct programming of nonvolatile memory cells] [N1203]

G11C16/34V4D . . . . . [N: Circuits or methods to detect overprogrammed nonvolatile memory cells, usually during program verification] [N1203]

G11C16/34V6 . . . . . [N: Prevention of overerasure or overprogramming, e.g. by verifying whilst erasing or writing] [N0107]

G11C16/34V6E . . . . . [N: Circuits or methods to verify correct erasure of nonvolatile memory cells whilst erasing is in progress, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate erasure] [N1206]

G11C16/34V6F . . . . . [N: Circuits or methods to prevent overerasing of nonvolatile memory cells, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate erasing] [N1203]

G11C16/34V6P . . . . . [N: Circuits or methods to verify correct programming of nonvolatile memory cells whilst programming is in progress, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate programming] [N1203]

G11C16/34V6Q . . . . . [N: Circuits or methods to prevent overprogramming of nonvolatile memory cells, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate programming] [N1203]

G11C16/34W . . . . [N: Arrangements for evaluating degradation, retention or wearout, e.g. by counting erase cycles] [N0107]

G11C16/34W2 . . . . . [N: Circuits or methods to detect or delay wearout of nonvolatile EPROM or EEPROM memory devices, e.g. by counting numbers of erase or reprogram cycles, by using multiple memory areas serially or cyclically] [N1203]

G11C17/00 **Read-only memories programmable only once; Semi-permanent stores, e.g. manually-replaceable information cards** ([N: multibit read-only memories G11C11/56R;] erasable programmable read-only memories G11C16/00; coding, decoding or code conversion, in general H03M; [N: combination of ROM and RAM G11C11/00C, G11C14/00; for electrical control of combustion engines F02D41/24D]) [C0210]

G11C17/00B . [N: with a storage element common to a large number of data, e.g. perforated card (G11C17/02, G11C17/04 take precedence)]

G11C17/02 . using magnetic or induction elements (G11C17/14 takes precedence)

G11C17/04 . using capacitive elements (G11C17/06, G11C17/14 take precedence)

G11C17/06 . using diode elements (G11C17/14 takes precedence)

G11C17/08 . using semiconductor devices, e.g. bipolar elements (G11C17/06, G11C17/14 take precedence)

G11C17/10 . . in which contents are determined during manufacturing by a predetermined arrangement of coupling elements, e.g. mask-programmable ROM

G11C17/12 . . . using field-effect devices

G11C17/12N . . . . [N: comprising cells having several storage transistors connected in series] [N9410]

G11C17/12V . . . . [N: Virtual ground arrays] [N9410]

G11C17/14 . in which contents are determined by selectively establishing, breaking or modifying connecting links by permanently altering the state of coupling elements, e.g. PROM

G11C17/14L . . [N: using laser-fusible links] [N1203]

G11C17/14W . . [N: Write once memory, i.e. allowing changing of memory content by writing additional bits] [N1203]

G11C17/16 . . using electrically-fusible links

G11C17/16R . . . [N: Memory cells which are electrically programmed to cause a change in resistance, e.g. to permit multiple resistance steps to be programmed rather than conduct to or from non-conduct change of fuses and antifuses (digital stores using resistance random access memory elements G11C13/00R)] [N1203]

G11C17/18 . . Auxiliary circuits, e.g. for writing into memory (in general G11C7/00)

G11C19/00 **Digital stores in which the information is moved stepwise, e.g. shift register** (counting chains H03K23/00) [N: stack stores, push-down stores (linear pulse counters H03K23/02, pulse distributors H03K5/15, methods and arrangements for shifting data G06F5/01)]

G11C19/00D . [N: with ferro-electric elements (condensers)]

G11C19/02 . using magnetic elements (G11C19/14 takes precedence)

G11C19/04 . . using cores with one aperture or magnetic loop

G11C19/06 . . using structures with a number of apertures or magnetic loops, e.g. transfluxors [N: laddic]

G11C19/08 . . using thin films in plane structure [N: thin magnetic films and apparatus or processes specially adapted for manufacturing or assembling the same H01F10/00, H01F41/14]

G11C19/08C . . . [N: using magnetic domain propagation]

G11C19/08C2 . . . . [N: using a rotating or alternating coplanar magnetic field]

G11C19/08C4 . . . . [N: using a variable perpendicular magnetic field]

G11C19/08C6 . . . . [N: using magnetic domain interaction]

G11C19/08C8 . . . . [N: using electric current]

G11C19/08D . . . [N: Generating magnetic fields therefor, e.g. uniform magnetic field for magnetic domain stabilisation (coil construction H01F5/00; electromagnets H01F7/06)]

G11C19/08E . . . [N: Generating, replicating or annihilating magnetic domains (also comprising different types of magnetic domains, e.g. "Hard Bubbles") (G11C19/08F takes precedence)]

G11C19/08F . . . [N: Detecting magnetic domains (measuring or detecting magnetic fields in general G01R33/02)]

G11C19/08G . . . [N: Organisation of a plurality of magnetic shift registers (FIFO`s G06F5/06, LIFO`s G06F7/78)] [C9807]

G11C19/08G2 . . . . [N: Means for switching magnetic domains from one path into another path, i.e. transfer switches, swap gates, decoders... (logic circuits using magnetic domains H03K19/168)]

G11C19/08G2H . . . . . [N: using hybrid structure, e.g. ion doped layers]

G11C19/10 . . using thin films on rods; with twistors

G11C19/12 . using non-linear reactive devices in resonant circuits, [N: e.g. parametrons; magnetic amplifiers with overcritical feedback]

G11C19/14 . using magnetic elements in combination with active elements, e.g. discharge tubes, semiconductor elements [N: contains no documents, see provisionally G11C19/02 to G11C19/10]

G11C19/18 . using capacitors as main elements of the stages [N: if capacitors are used as auxiliary stage in between main stages with other elements, the latter take precedence; G11C19/00D takes precedence]

G11C19/18B . . [N: in combination with semiconductor elements, e.g. bipolar transistors, diodes]

G11C19/18B2 . . . [N: with field-effect transistors, e.g. MOS-FET]

G11C19/18B2B . . . . [N: using only one transistor per capacitor, e.g. bucket brigade shift register]

G11C19/18B4 . . . [N: Organisation of a multiplicity of shift registers, e.g. regeneration, timing, input-output circuits (FIFO`s G06F5/06; LIFO`s G06F7/78)]

G11C19/20 . using discharge tubes (G11C19/14 takes precedence)

G11C19/20B . . [N: with vacuum tubes (G11C19/20D takes precedence)]

G11C19/20C . . [N: with gas-filled tubes (G11C19/20D takes precedence)]

G11C19/20D . . [N: with counting tubes]

G11C19/28 . using semiconductor elements (G11C19/14 takes precedence)

G11C19/28B . . [N: with charge storage in a depletion layer, i.e. charge coupled devices (C.C.D)]

G11C19/28B2 . . . [N: Peripheral circuits, e.g. for writing into the first stage; for reading-out of the last stage]

G11C19/28C . . [N: Organisation of a multiplicity of shift registers (FIFO`s G06F5/06, LIFO`s G06F7/78)]

G11C19/30 . using opto-electronic devices, i.e. light emitting and photoelectric devices electrically or optically coupled

G11C19/32 . using super-conductive elements

G11C19/34 . using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency [N: (in RAM multistable cells G11C11/56; in

capacitive analog stores G11C27/04)] [N0506]

G11C19/36 . . using [N: multistable] semiconductor elements [N0506]

G11C19/38 . two-dimensional, e.g. horizontal and vertical shift registers [N0506]

G11C21/00 **Digital stores in which the information circulates** [N: continuously] (stepwise G11C19/00)

G11C21/00B . [N: using electrical delay line (construction of such lines H03H7/30, H03H11/26)]

G11C21/02 . using electromechanical delay lines, e.g. using a mercury tank [N: construction of such lines H03H9/00]

G11C21/02B . . [N: using piezo-electric transducers, e.g. mercury tank]

G11C21/02D . . [N: using magnetostriction transducers, e.g. nickel delay line]

G11C23/00 **Digital stores characterised by movement of mechanical parts to effect storage, e.g. using balls; Storage elements therefor** (storing by actuating contacts G11C11/50)

G11C25/00 **Digital stores characterised by the use of flowing media; Storage elements therefor** [N: (multiple fluid-circuit element arrangements for performing digital operations F15C1/12)]

G11C27/00 **Electric analogue stores, e.g. for storing instantaneous values** [N: (integrating circuits acting as stores G06G7/18; pulse counters with step by step integration and static storage H03K25/00)]

G11C27/00F . [N: with non-volatile charge storage, e.g. on floating gate or MNOS]

G11C27/02 . Sample-and-hold arrangements (G11C27/04 takes precedence; sampling electrical signals, in general H03K)

G11C27/02B . . [N: using a magnetic memory element]

G11C27/02C . . [N: using a capacitive memory element (G11C27/04 takes precedence)]

G11C27/02C1 . . . [N: associated with an amplifier (G11C27/02C2 takes precedence)] [C9708]

G11C27/02C2 . . . [N: Current mode circuits, e.g. switched current memories] [N9708]

G11C27/04 . Shift registers (charge coupled devices per se H01L29/76)

G11C29/00 **Checking stores for correct operation;** [N: Subsequent repair]**; Testing stores during standby or offline operation** [N: (testing of electronic circuits in general G01R31/28; error detection or error correction in computer memories during normal operation G06F11/10M, G06F11/16M; testing of computers during standby G06F11/22)] [C1004]

[N: **WARNING**
[N1111] Groups G11C29/70 to G11C29/886 do not correspond to former or current IPC groups.
Concordance ECLA : IPC for these groups is the following: - G11C29/70 - G11C29/886 : G11C29/00
]

G11C29/00S . [N: in serial memories]

G11C29/00W . [N: at wafer scale level, i.e. WSI (for test and configuration during manufacture H01L22/00)] [N0203] [M1205]

G11C29/02 . Detection or location of defective auxiliary circuits, e.g. defective refresh counters [N0505]

G11C29/02A . . [N: in voltage or current generators] [N1205]

G11C29/02B . . [N: in I/O circuitry] [N1205]

G11C29/02C . . [N: in clock generator or timing circuitry] [N1205]

G11C29/02D . . [N: in decoders] [N1205]

G11C29/02E . . [N: in signal lines] [N1205]

G11C29/02F . . [N: in sense amplifiers] [N1205]

G11C29/02G . . [N: in fuses] [N1205]

G11C29/02H . . [N: with adaption or trimming of parameters] [N1205]

G11C29/04 . Detection or location of defective memory elements, [N: e.g. cell constructio details, timing of test signals] [N0505]

G11C29/06 . . Acceleration testing [N0505]

G11C29/08 . . Functional testing, e.g. testing during refresh, power-on self testing (POST) or distributed testing [N0505]

G11C29/10 . . . Test algorithms, e.g. memory scan (MScan) algorithms; Test patterns, e.g. checkerboard patterns [N0505]

G11C29/12 . . . Built-in arrangements for testing, e.g. built-in self testing (BIST) [N: or interconnection details] [N0505]

G11C29/12A . . . . [N: comprising voltage or current generators] [N1205]

G11C29/12B . . . . [N: comprising I/O circuitry] [N1205]

G11C29/12C . . . . [N: comprising clock generation or timing circuitry] [N1205]

G11C29/14 . . . . Implementation of control logic, e.g. test mode decoders [N0505]

G11C29/16 . . . . . using microprogrammed units, e.g. state machines [N0505]

G11C29/18 . . . . Address generation devices; Devices for accessing memories, e.g. details of addressing circuits [N0505]

G11C29/20 . . . . . using counters or linear-feedback shift registers (LFSR) [N0505]

G11C29/22 . . . . . Accessing serial memories [N0505]

G11C29/24 . . . . . Accessing extra cells, e.g. dummy cells or redundant cells [N0505]

G11C29/26 . . . . . Accessing multiple arrays (G11C29/24 takes precedence) [N0505]

G11C29/28 . . . . . Dependent multiple arrays, e.g. multi-bit arrays [N0505]

G11C29/30 . . . . . Accessing single arrays [N0505]

G11C29/32 . . . . . Serial access; Scan testing [N0505]

G11C29/34 . . . . . Accessing multiple bits simultaneously [N0505]

G11C29/36 . . . . Data generation devices, e.g. data inverters [N0505]

G11C29/38 . . . . Response verification devices [N0505]

G11C29/40 . . . . . using compression techniques [N0505]

G11C29/42 . . . . . using error correcting codes (ECC) or parity check [N0505]

G11C29/44 . . . . Indication or identification of errors, e.g. for repair [N0505]

G11C29/44A . . . . . [N: for self repair] [N1205]
G11C29/46 . . . . Test trigger logic [N0505]
G11C29/48 . . . Arrangements in static stores specially adapted for testing by means external to the store, e.g. using direct memory access (DMA) or using auxiliary access paths (external testing equipment G11C29/56) [N0505]
G11C29/50 . . Marginal testing, e.g. race, voltage or current testing [N0505]
G11C29/50A . . . [N: of threshold voltage] [N1205]
G11C29/50B . . . [N: of impedance] [N1205]
G11C29/50C . . . [N: of timing] [N1205]
G11C29/50D . . . [N: of retention] [N1205]

G11C29/52 . Protection of memory contents; Detection of errors in memory contents [N0505]

G11C29/54 . Arrangements for designing test circuits, e.g. design for test (DFT) tools [N0505]

G11C29/56 . External testing equipment for static stores, e.g. automatic test equipment (ATE); Interfaces therefor [N0505]
G11C29/56A . . [N: Pattern generation] [N1205]
G11C29/56B . . [N: Error analysis, representation of errors] [N1205]
G11C29/56C . . [N: Timing aspects, clock generation, synchronisation] [N1205]
G11C29/56D . . [N: Apparatus features] [N1205]

G11C29/70 . [N: Masking faults in memories by using spares or by reconfiguring] [N1111]
G11C29/702 . . [N: by replacing auxiliary circuits, e.g. spare voltage generators, decoders or sense amplifiers, to be used instead of defective ones] [N1111]
G11C29/72 . . [N: with optimized replacement algorithms] [N1111]
G11C29/74 . . [N: using duplex memories, i.e. using dual copies] [N1111]
G11C29/76 . . [N: using address translation or modifications] [N1111]
G11C29/765 . . . [N: in solid state disks] [N1111]
G11C29/78 . . [N: using programmable devices] [N1111]
G11C29/781 . . . [N: combined in a redundant decoder] [N1111]
G11C29/783 . . . [N: with refresh of replacement cells, e.g. in DRAMs] [N1111]
G11C29/785 . . . [N: with redundancy programming schemes] [N1111]
G11C29/787 . . . . [N: using a fuse hierarchy (for memories using fuses in general G11C17/16)] [N1111]
G11C29/789 . . . . [N: using non-volatile cells or latches (erasable programmable memory cells in general G11C16/00)] [N1111]
G11C29/80 . . . [N: with improved layout] [N1111]
G11C29/802 . . . . [N: by encoding redundancy signals] [N1111]
G11C29/804 . . . . [N: to prevent clustered faults] [N1111]
G11C29/806 . . . . [N: by reducing size of decoders] [N1111]
G11C29/808 . . . . [N: using a flexible replacement scheme] [N1111]
G11C29/81 . . . . [N: using a hierarchical redundancy scheme] [N1111]
G11C29/812 . . . . [N: using a reduced amount of fuses] [N1111]
G11C29/814 . . . . [N: for optimized yield] [N1111]

G11C29/816 . . . . [N: for an application-specific layout] [N1111]
G11C29/818 . . . . . [N: for dual-port memories] [N1111]
G11C29/82 . . . . . [N: for EEPROMs] [N1111]
G11C29/822 . . . . . [N: for read only memories] [N1111]
G11C29/824 . . . . . [N: for synchronous memories] [N1111]
G11C29/83 . . . [N: with reduced power consumption] [N1111]
G11C29/832 . . . . [N: with disconnection of faulty elements] [N1111]
G11C29/835 . . . [N: with roll call arrangements for redundant substitutions] [N1111]
G11C29/838 . . . [N: with substitution of defective spares] [N1111]
G11C29/84 . . . [N: with improved access time or stability] [N1111]
G11C29/842 . . . . [N: by introducing a delay in a signal path] [N1111]
G11C29/844 . . . . [N: by splitting the decoders in stages] [N1111]
G11C29/846 . . . . [N: by choosing redundant lines at an output stage] [N1111]
G11C29/848 . . . . [N: by adjacent switching] [N1111]
G11C29/86 . . [N: in serial access memories, e.g. shift registers, CCDs, bubble memories] [N1111]
G11C29/88 . . [N: with partially good memories] [N1111]
G11C29/883 . . . [N: using a single defective memory device with reduced capacity e.g. half capacity] [N1111]
G11C29/886 . . . [N: combining plural defective memory devices to provide a contiguous address range e.g. one device supplies working blocks to replace defective blocks in another device] [N1111]

G11C99/00 **Subject matter not provided for in other groups of this subclass** [N0704]