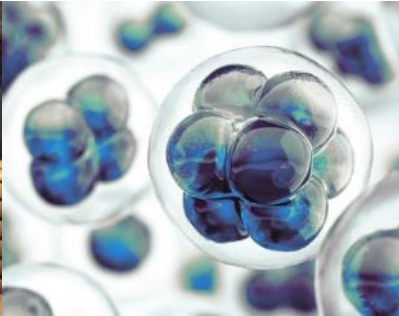




Europäisches
Patentamt
European
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Utilization of AI at EPO



EPO is focusing on



Classification



Automated Search



Machine Translation



Decision support

Programme Breakdown



Simplify and modernise IT Systems

KPI2.1
Availability of existing and new tools

KPI2.2
Processes digitalised

KPI2.3
Users' satisfaction with tools

Artificial Intelligence Essentials

Computer Vision

- Patent figures
- Facsimiles parsing e.g. tables
- Understanding figure content

KPI3.2
Quality of search and examination (%)
(Internal Audit)

Natural Language Processing

- Managing patent language
- Patent syntax in general
- e.g. claim syntax specifically

KPI3.2
Quality of search and examination (%)
(Internal Audit)

Machine Translation

- Specific to our business needs
- Build on patent content
- Proven to improve PreSearch/PreCla

KPI3.2
Quality of search and examination (%)
(Internal Audit)

(19) Deutsches Patent- und Markenamt

(10) DE 10 2017 212 839 A1 2019.01.31

(12) **Offenlegungsschrift**

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(22) Anmeldetag: 26.07.2017 G06F 11/40 (2006.01)
(43) Offenlegungstag: 31.01.2019

(71) Anmelder: Robert Bosch GmbH, 70469 Stuttgart, DE (72) Erfinder: Kleemann, Raf, 71726 Benningen, DE

Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen.

(54) Bezeichnung: **Kontrollmodul für Künstliche Intelligenz**

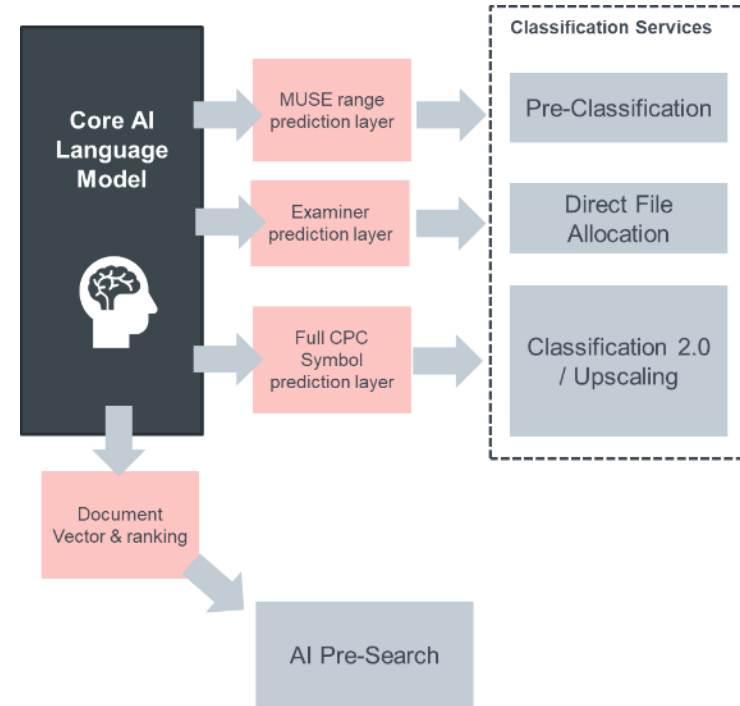
(57) Zusammenfassung: Kontrollmodul (3) für ein System (1), das eine oder mehrere Eingangsgrößen (11) mit einem Künstliche-Intelligenz-Modul, KI-Modul (2), in eine oder mehrere Ausgangsgrößen (21) übersetzt, wobei die Ausgangsgröße (21) von einem Ausgang (23) des KI-Moduls (2) sowohl zu einem Ausgang (13) des Systems (1) geführt ist als auch als Rückkopplung in einen Eingang (22) des KI-Moduls (2) zurückgeführt ist, wobei das Kontrollmodul (3) einen Eingang (31), der mit dem Ausgang (23) des KI-Moduls (2) verbunden ist, und einen Ausgang (32), der mit dem Ausgang (13) des Systems (1) verbunden ist, aufweist und dazu ausgebildet ist, einen an seinem Eingang (31) empfangenen Wert der Ausgangsgröße (21) des KI-Moduls (2) nur dann an seinen Ausgang (32) weiterzugeben, wenn dieser Wert mindestens einer in dem Kontrollmodul (3) hinterlegten Randbedingung (33) genügt.

System (1), das eine oder mehrere Eingangsgrößen (11) mit einem Künstliche-Intelligenz-Modul, KI-Modul (2), in eine oder mehrere Ausgangsgrößen (21) übersetzt, wobei die Ausgangsgröße (21) von einem Ausgang (23) des KI-Moduls (2) sowohl zu einem Ausgang (13) des Systems (1) geführt ist als auch als Rückkopplung in einen Eingang (22) des KI-Moduls (2) zurückgeführt ist, wobei ein Kontrollmodul (3) vorgesehen ist, wobei der Eingang (31) des Kontrollmoduls (3) mit einem Ausgang (23) des KI-Moduls (2) und der Ausgang (32) des Kontrollmoduls (3) mit einem Ausgang (13) des Systems (1) verbunden ist.

Zugehöriges

Natural Language Processing Project

- Patent language is different
- Our tasks are very specific (file allocation, prior art search, etc)
- No off-the-shelf solutions
- **Our approach**
 - Adapt most promising available NLP AI models to patent language (BERT)
 - Understand & own AI components



Full Classification – from meta data to annotation

EP3151272A1

Title: Semiconductor device and method of manufacturing semiconductor device

CPC: H01L21/31 H01L21/31056 (+80)

Pub. Date: 2017-03-30

Pages: 13 (double column)

Example: [H01L2924/13091](#) (TP)

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

[H01L2224/04042](#) (TP)

Bonding areas specifically adapted for wire connectors, e.g. wirebond pads

[H01L 2224/05624](#) (FP)

Aluminium [Al] as principal constituent

The screenshot displays a patent database interface with a left sidebar containing classification codes (A, B, C, D, E, F, G) and a main content area. The main content area is divided into sections: 'First Embodiment', 'Description of Structure', and a list of paragraphs [0019] through [0026]. The right side of the interface features a cross-sectional diagram of a semiconductor device with a color-coded legend on the right and a vertical axis on the left. The legend includes various classification codes such as H01L2224/0101, H01L2224/0202, H01L2224/0303, H01L2224/0404, H01L2224/0505, H01L2224/0606, H01L2224/0707, H01L2224/0808, H01L2224/0909, H01L2224/1010, H01L2224/1111, H01L2224/1212, H01L2224/1313, H01L2224/1414, H01L2224/1515, H01L2224/1616, H01L2224/1717, H01L2224/1818, H01L2224/1919, H01L2224/2020, H01L2224/2121, H01L2224/2222, H01L2224/2323, H01L2224/2424, H01L2224/2525, H01L2224/2626, H01L2224/2727, H01L2224/2828, H01L2224/2929, H01L2224/3030, H01L2224/3131, H01L2224/3232, H01L2224/3333, H01L2224/3434, H01L2224/3535, H01L2224/3636, H01L2224/3737, H01L2224/3838, H01L2224/3939, H01L2224/4040, H01L2224/4141, H01L2224/4242, H01L2224/4343, H01L2224/4444, H01L2224/4545, H01L2224/4646, H01L2224/4747, H01L2224/4848, H01L2224/4949, H01L2224/5050, H01L2224/5151, H01L2224/5252, H01L2224/5353, H01L2224/5454, H01L2224/5555, H01L2224/5656, H01L2224/5757, H01L2224/5858, H01L2224/5959, H01L2224/6060, H01L2224/6161, H01L2224/6262, H01L2224/6363, H01L2224/6464, H01L2224/6565, H01L2224/6666, H01L2224/6767, H01L2224/6868, H01L2224/6969, H01L2224/7070, H01L2224/7171, H01L2224/7272, H01L2224/7373, H01L2224/7474, H01L2224/7575, H01L2224/7676, H01L2224/7777, H01L2224/7878, H01L2224/7979, H01L2224/8080, H01L2224/8181, H01L2224/8282, H01L2224/8383, H01L2224/8484, H01L2224/8585, H01L2224/8686, H01L2224/8787, H01L2224/8888, H01L2224/8989, H01L2224/9090, H01L2224/9191, H01L2224/9292, H01L2224/9393, H01L2224/9494, H01L2224/9595, H01L2224/9696, H01L2224/9797, H01L2224/9898, H01L2224/9999.

First Embodiment
[0019] A structure of a semiconductor device of a first embodiment is now described with reference to drawings.

Description of Structure
[0020] Fig 1 is a section view illustrating a configuration of the semiconductor device of the first embodiment. The semiconductor device of the first embodiment includes a semiconductor substrate S, an interlayer insulating film IL1 provided on the semiconductor substrate S, and an interconnection M1 provided on the interlayer insulating film IL1. A semiconductor element is provided on the main surface of the semiconductor substrate S while being not shown in Fig. 1. For example, the interconnection M1 is electrically coupled to the semiconductor element via a plug P1.

[0021] Protective films PRO1 and PRO2 each including an insulating film are provided over the interconnection M1. The protective film PRO1 has an opening OA1, and part of the interconnection M1 is exposed from the bottom of the opening OA1. Such an exposed portion of the interconnection M1 is referred to as pad region PD. The protective film PRO2 has an opening OA2 that is disposed on the opening OA1 and a size larger than the opening OA1.

[0022] The interconnection M1 includes an aluminum film (Al film), for example. In other words, the interconnection M1 contains aluminum. The Al film described herein is not limited to pure Al film, and is a conductive material film (showing metallic conduction however) mainly containing aluminum. The Al film therefore includes a compound film or an alloy film of aluminum (Al) and silicon (Si), for example. A compositional ratio of Al in that film is desirably larger than 50 atomic percent.

[0023] The protective film PRO1 includes a silicon oxynitride film, for example. Not only the silicon oxynitride film but also a silicon oxide film or a silicon nitride film may be used as the protective film (cover film) PRO1. The protective film PRO2 includes a polyimide film, for example.

[0024] A plating film OPM1 is provided over the pad region PD as the bottom of the opening OA1. A plating film OPM2 is provided over the plating film OPM1. The plating film OPM1 includes a nickel (Ni) film, for example. The Ni film is formed over the pad region PD by electroless plating. The plating film OPM2 includes a gold (Au) film, for example. The Au film is formed over the plating film OPM1 by electroless plating. The plating films OPM1 and OPM2 may each be referred to as "over-pad metal" or "over-pad metal electrode (OPM electrode)" because such a plating film cover the pad region PD.

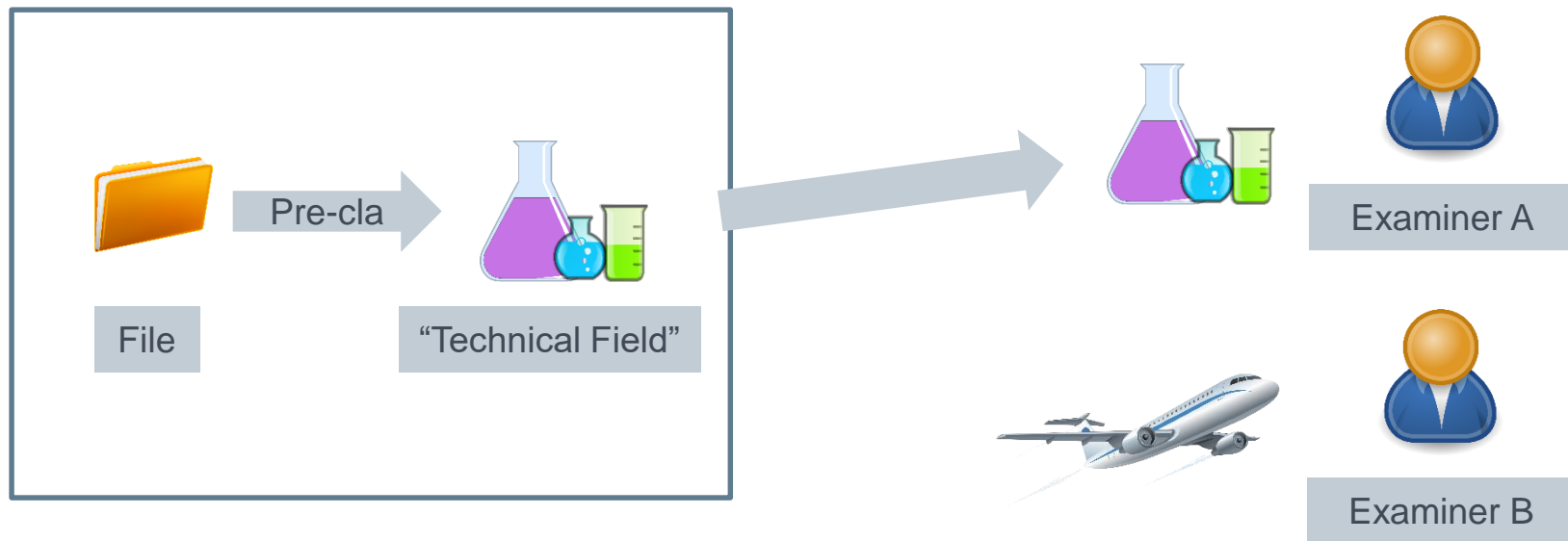
[0025] For example, the plating film OPM1 is provided to suppress formation of an undesired metal compound caused by direct contact of a bonding wire (conductive wire) described later to the pad region PD. For example, the plating film OPM2 is provided to improve adhesion of the bonding wire (conductive wire) described later to the plating film OPM1.

[0026] In the first embodiment, a slit (side slit, recess) SL is provided in a side face of the opening OA1. In Fig. 1, the slit SL is provided in a bottom portion of the side face of the opening OA1. The slit SL can be a portion of the side face retreated to the outside of the opening OA1. In this exemplary case, the slit SL has a tapered shape. From another perspective, the opening OA1 has an open region larger in its bottom than in its top. In Fig. 1, the open region in the bottom is a size larger than the open region in the top. The plating film OPM1 is also provided in the slit SL.

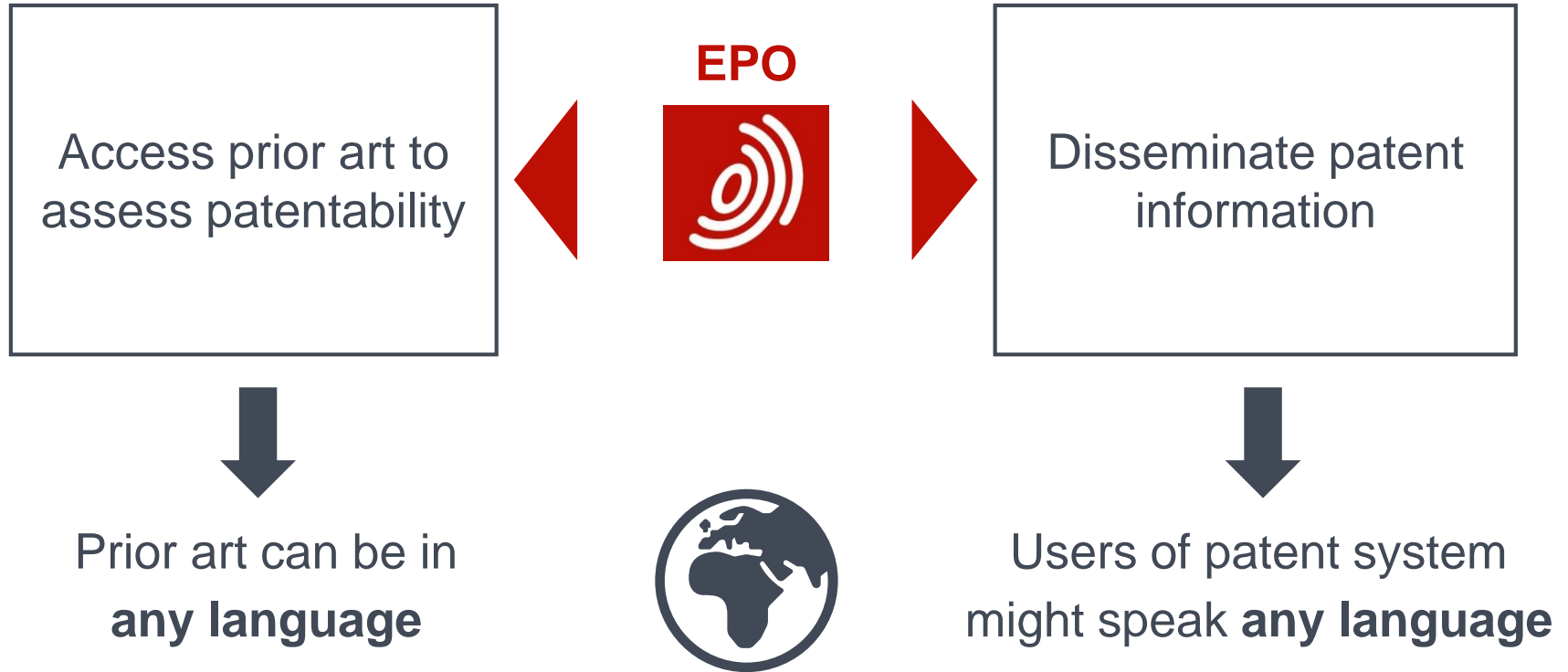
The pre-classification task

- Pre-classification

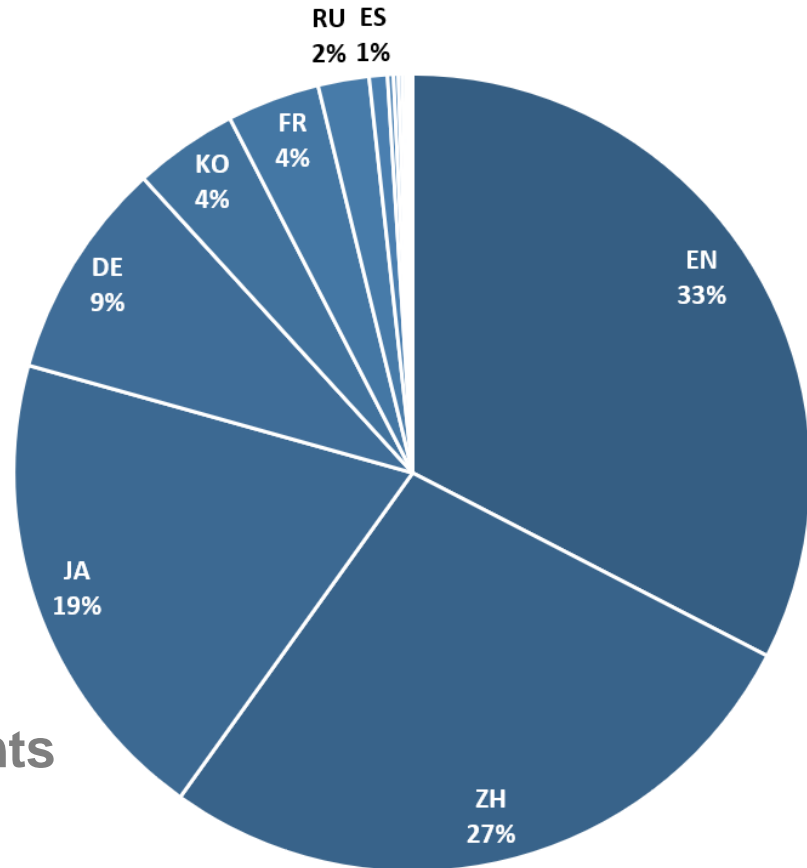
- Goal: map a new patent application to a (technically) competent examiner
- A key decision for high quality search & examination



Machine Translation at the EPO: motivation



Documents per language in EPO collection



100M Full-text documents

Development of MT engines in-house

- Engines for translation of non-published applications
 - English ↔ German, French, Dutch, Italian
- Development of custom engines for patent language
 - Specialization by technical field
 - Specialization by document section (title, description & abstract, claims)
- Development of engines for low-resourced languages

Thank you very much for your attention!